

Design of Equal Precision Frequency Meter Based on FPGA*

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ABSTRACT

To overcome the shortcoming that the traditional frequency measurement method does not meet the requirement of equal precision, a design method of equal precision frequency meter based on FPGA is proposed. The system modules are all realized in Altera's FPGA chip EP2C35F672C8. Experimental results show that the system can measure frequencies with equal precision in the whole frequency range, and the measurement error is small. It achieves the requirement of equal precision measurements.

Keywords: FPGA; Equal Precision; Frequency Measurement

1. Introduction

Frequency measurement is one of the most basic and important method in electronic measurements. Frequency signals are strong anti-interference, easy to transmit, and can be measured with higher precision. Therefore, the study of frequency measurement method is important in the practical engineering applications. The commonly used frequency measurement methods are direct frequency measurement, direct period measurement, and equal precision frequency measurement, etc. Direct frequency measurement is the method that counts the pulse number N within time t , then calculates the pulse number per unit time, *i.e.*, the frequency of measured signal. Direct period measurement is the method that first measures the period T of the measured signal, then calculates the signal frequency by $f = 1/T$. However, these two methods will produce ± 1 period error of the measured signal, and therefore have some limitations in practical applications. According to the measurement principle, it is very easy to find that the frequency measurement method is suitable for high-frequency signal, and period measurement method is suitable for low-frequency signal, however, both can not take into account the requirement of equal precision measurement of high and low frequencies [1]. The maximum advantage of equal precision frequency measurement method compared to other frequency measurement methods is that it can achieve the equal precision in the entire frequency range, and have nothing to do with the size of the signal frequency.

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2. Principle of Equal Precision Frequency Measurement

The equal precision frequency measurement is also known as multi-cycle synchronous frequency measurement method. Its most prominent feature is that the actual gate time is not a fixed value, but a value related with the measured signal, it is exactly an integer multiple of the measured signal period. Within the time allowed counting, we count pulse numbers of the standard signal and the measured signal at the same time, then derive the frequency of the measured signal through mathematical formula. As the gate time is an integer multiple of the measured signal period, this eliminates the ± 1 period error of the measured signal, however, it will produce the ± 1 period error of the standard signal [2]. The schematic diagram of equal precision measurement is shown in **Figure 1**.

First, the control circuit gives out the gate signal, but the counter does not start counting until the rising edge of the measured signal comes. Then, the two counters start counting the pulse numbers of the measured signal and the standard signal respectively, and end counting until the falling edge of the measured signal, thus complete one measurement process. The counter's opening and ending is completely synchronized with the measured signal.

Figure 1 shows that the actual gate time is not a fixed value, it is exactly an integer multiple of the measured signal period, and it is synchronized with the measured signal. This eliminates the ± 1 period error of the measured signal. From the principle of frequency measure

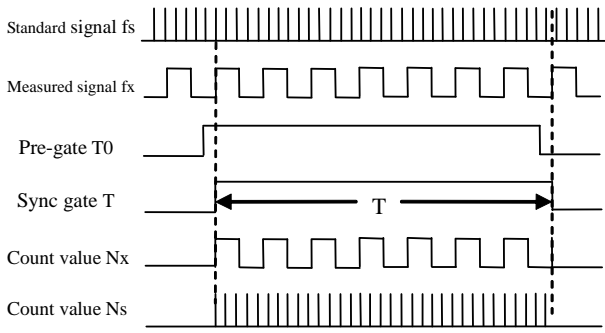


Figure 1. Schematic diagram of equal precision measurement.

ment, we can obtain:

$$T = \frac{N_x}{f_x} = \frac{N_s}{f_s} \quad (1)$$

After deformation, we obtain:

$$f_x = \frac{N_x}{N_s} f_s \quad (2)$$

Differentiating to the above equation, obtain:

$$df_x = \frac{f_s}{N_s} dN_x - \frac{N_x}{N_s^2} f_s dN_s + \frac{N_x}{N_s} df_s \quad (3)$$

For $dN_x = 0$, $dN_s = \pm 1$, and $\frac{N_x}{f_x} = \frac{N_s}{f_s}$

Thus:

$$\frac{df_x}{f_x} = \pm \frac{1}{N_s} + \frac{df_s}{f_s} \quad (4)$$

From (4) we can see: the measurement error has nothing to do with the frequency of the measured signal, only related with the gate time and frequency of standard signals, namely, the equal precision measuring was achieved within the measured frequency band. The longer the gate time T and the higher the standard frequency f_s , the smaller relative error of the measured frequency. The relative error of standard frequency is df_s/f_s . Because the stability of the crystal is very high, therefore, the relative error of the standard signal is very small, and can be ignored.

3. Implementations of Equal Precision Frequency Meter

The core idea of equal precision measurement is how to ensure the actual gate time is an integer multiple of the measured signal cycle. This requires the design to establish a certain relationship between the actual gate time and the measured signal [3]. Based on this idea, the design lets the rising edge of the measured signal as the drive signal for the gate opening and closing. Only when

the rising edge of the measured signal reaches, the state of the pre-gate T_0 is latched, so that the cycles of the measured signal during the actual measurement gate (*i.e.* synchronous gate T) is an integer. The block diagram of equal precision frequency is shown in **Figure 2**.

In **Figure 2**, the preset GATE signal is produced by a timing module in FPGA. Here the length of the preset gate signal is 1 s [4]. CNT1 and CNT2 are two controlled 32-bit high-speed counters. CNT1_ENA and CNT2_ENA are their count enable terminals respectively. The reference frequency signal f_s is input to CNT1_CLK. The measured signal f_x is input to CNT2_CLK, and also connected to the clk of D flip-flop. During measurement, the timing module in FPGA generates preset GATE signal. When GATE is in high level, and at the rising edge of f_x , the 2 counters are triggered and start to count the reference signal and the measured signal respectively. The condition for closing the counting gate is: GATE is low, and at the rising edge of f_x . If in an actual gate time T_x , the count value of the measured signal is N_x , and the count value of the standard signal is N_s , then by formula (2), the frequency of measured signal f_x can be calculated: $f_x = (N_x/N_s)*f_s$. For example, the counts of standard signal and measured signal are 220 and 11, according to equation (2), if the standard signal frequency is 20 MHz, then the measured signal frequency equals $(11/220) \times 20$ MHz = 1 MHz.

3.1. System Design

The 50 MHz clock in the development platform is selected as the system clock of this experiment. The gate time is taken as 1 s (obtained by dividing the system clock). The enable signal TSTEN is a periodic signal with pulse width of 1 s, which is used to synchronize the two decimal counters CNT10. The counter is enabled when TSTEN is high, and disabled when it is low. During the disabled period, a rising edge of the latch signal LOAD is needed to latch the count value of the previous second into a 32-bit REG32B. The count value is translated by the decoder and displayed stable by seven-segment display. After latching, the counter is

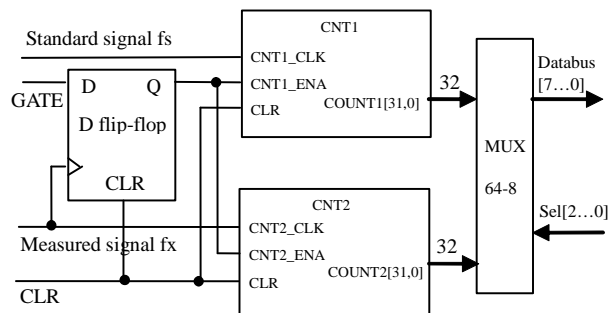


Figure 2. Block diagram of equal precision frequency.

cleared by the clear signal CLR_CNT, and prepared for the next counting.

The frequency number N_x of the measured signal f_x is obtained by the cascade of eight decimal counter CNT10, and so does the standard signal frequency N_s . The completed count data is sent to the latch module REG32B for saving.

In this study, the system development platform provides eight seven-segment displays, it can display up to 99,999,999. Therefore, the measurement range is 0 - 100 MHz. The display module is represented by eight 4-bit binary code (BCD code). It outputs the data of the latch (REG32B) to the display module, and displays it by the seven-segment LED. Data latch is to ensure that the system can stabilize the display data. The decoder driver circuit is used to convert the binary count results into decimal results which can be displayed with seven-segment LED.

The system block diagram is shown in **Figure 3**. It mainly consists of six modules, namely: source module, signal selection module, control module, counting module, latch module and decoding display module.

3.2. Module Design and Function Simulation

3.2.1. Source Module

The source module includes a pre frequency division module, and a multi frequency division module. In this paper, they are implemented with VHDL language. The pre frequency division module divides the input system clock (50 MHz) to generate a 1MHz clock frequency signal. Its timing simulation is shown in **Figure 4**. From **Figure 4**, we can see a 1 MHz clock frequency is generated by dividing the 50 MHz system clock with 50, which achieving the desired effect of the design.

The frequency divider module CNT has the function of generating variety of signals. Its main function is to

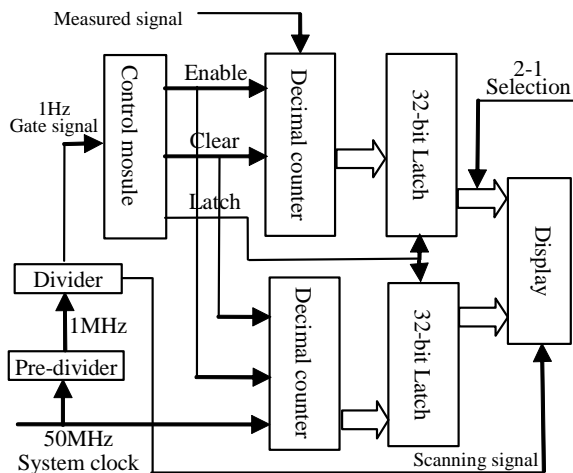


Figure 3. System block diagram.

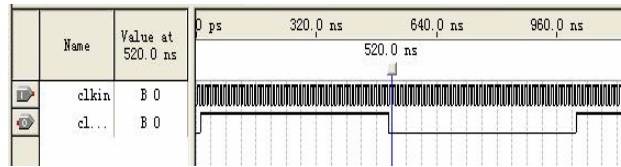


Figure 4. Simulation of pre frequency division.

produce a gate signal with 1 s pulse width, a 7812 Hz scanning signal, and other desired test signals, including 500 KHz, 125 KHz, 31250 Hz, 7812 Hz, 1953 Hz, 488 Hz, and 1 Hz output frequencies. The input signal CLK is 1 MHz, the 1 Hz output signal freq1 is sent to the control module, and the 7812 Hz output frequency is used as the input scanning signal of the display module. The other frequencies are used as test signals. The simulation of the frequency divider is shown in **Figure 5**.

3.2.2. Control Module

The role of the control module is to produce a variety of required control signals for measuring frequency. Its input clock is 1 Hz, measuring the frequency once every two clock cycles. The input terminal CLK is connected to the output freq 1 of the divider CNT. The control module generates three control signals, respectively, CLR_CNT TSTEN, and LOAD. The CLR_CNT signal is used to reset the counter at the beginning of each counting to clear the last count result, which is connected to CLR of the counter CNT10, high level effective, and sustains half a clock cycle. TSTEN is the count enable signal, is connected to ENA of the counter CNT10. At the rising edge of TSTEN, the count module starts to count the frequency of the input signal. The counting time is exactly one clock cycle (*i.e.* one unit time 1 s). The count value among this time is the signal frequency. The output terminal LOAD is connected to the latch's input terminal LOAD. The simulation diagram of the control module is shown in **Figure 6**.

In the figure, the control signal clock CLK is taken as 1 Hz, therefore, the pulse width of TSTEN is just 1 s, which can be used as a gate signal. The figure also shows that the enable signal TETEN lasts 1 s in high level before the counting finished, then its opposite latch signal LOAD produces a rising edge, and after 0.5 s, the clear signal CLR_CNT produces a rising edge.

3.2.3. Decimal Counter

The counter module is cascaded by eight decimal count module CNT10 with asynchronous clear and carry on signal. The special about this decimal counter is that it has a clock enable input terminal ENA which is used to lock the counter. The counter is allowed to count when ENA at high level, and prohibited to count at low level. The counter module is used to count the pulses of the input signal. The module must have count enable termi-

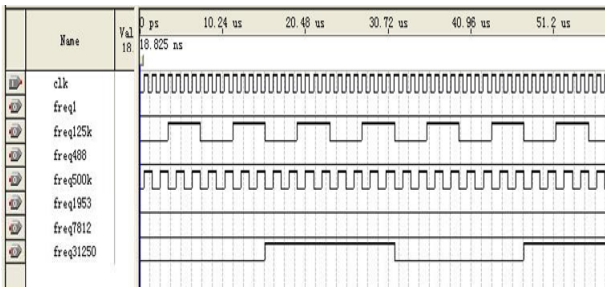


Figure 5. Simulation of frequency divider.

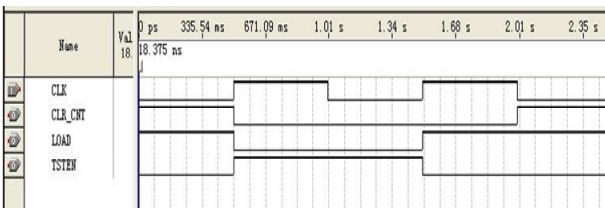


Figure 6. Simulation of control module.

nal and asynchronous clear terminal for the control module to control it.

The reset terminal CLR of CNT10 is connected to the output terminal CLR_CNT of TESTCTL, its enable terminal ENA is connected to the TSTEN terminal of TESTCTL, and its output terminal CQ[3..0] is connected to DIN[31..0] of the latch. The simulation is shown in Figure 7.

The function of this module is to realize a decimal counter with enable terminal. The counter works properly only when the enable signal is at high level. The counter pluses one when each rising edge of the clock comes. When counting to 10, the counter is cleared, while a carry on signal is produced, which is only a pulse signal. Once the count changes from 10 to 1, the pulse signal immediately goes low. Also the counter has a clear signal. Once the clear signal is at high level, the counter is cleared immediately. In this design, two signals need to be counted, so there are two 32-bit data output.

3.2.4. 32-Bit Latch

The latch module is mainly composed by the master-slave flip-flop. It plays the role of data protection to ensure its stability before being displayed. After the count module completes counting, the latch module latches the count value into the register at the rising edge of the load signal; then outputs to the display module, and save the data until the next trigger or reset.

The latch's input terminal LOAD is connected to the output terminal LOAD of the control module TESTCTL; its input terminal DIN[31..0] is connected to output terminal CQ[3..0] of the counter CNT10, and its output terminal DOUT[31..0] is connected to the In[3..0] terminals of the Display module.

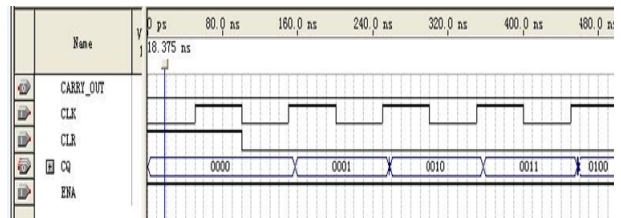


Figure 7. Simulation of CNT10.

3.2.5. Seven-Segment LED Display Module

Seven-segment LED has segment code and location code. Segment code is used to convert the 4-bit binary input number into the corresponding 8-bit segment code for LED display through a decoding circuit. Location code is used to enable the LED. For the common cathode LED, low level enables. This design uses a 3-bit circulating selector to enable each LED in turn. Because there are eight LED need to display simultaneously, we must cyclic scan each LED, and input the 8-bit segment code corresponding to the required display data while enable each LED. Although the 8 LED display in turn, but for the sake of visual resolution, it looks the 8 LED work simultaneously.

The block diagram of display module is shown in Figure 8. Where In0 - In7 is connected to DOUT[31..0] of the latch, and output terminals are connected to the segment and select pins of LED.

All modules in the design are implemented in Altera's FPGA chip EP2K35F672C8. The outputs of the counting modules are two 32-bit data. These two 32-bit data is output by the latch. The counting numbers N_x and N_s are converted into the actual frequency value according to the equal precision frequency Formula (2).

4. Experimental Results and Error Analysis

In experiment, the 50 MHz high stability quartz crystal was used as the standard signal. The measured results and relative errors are shown in Table 1.

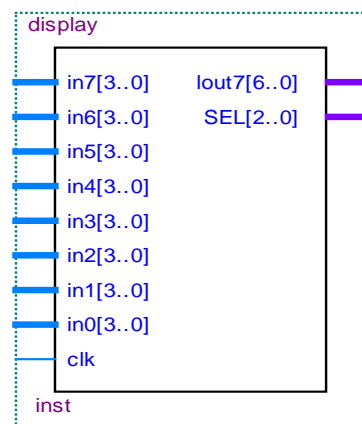


Figure 8. Block diagram of display module.

Table 1. Experimental result and relative errors.

Input Frequencies	N_x	N_s	Relative Errors
100 KHz	100000	50000000	2.000000×10^{-8}
1 MHz	1000007	50000350	1.999986×10^{-8}
6 MHz	6000044	50000365	1.999985×10^{-8}
12 MHz	12000077	50000320	1.999987×10^{-8}
24 MHz	24000154	50000320	1.999987×10^{-8}

The results show that the relative error is less than 2×10^{-8} within the experimental frequency range 100 KHz to 24 MHz. The measurement errors distribute in the same order of magnitude, which achieves the purpose of equal precision measurement.

5. Conclusion

This paper describes the principles of equal precision measuring, proposes the design method of precision frequency meter based on FPGA. Because the design can eliminate the ± 1 count error of the measured signal,

therefore, greatly improve the precision, and can achieve equal precision measurement without changing the measuring range in the whole frequency range. The results show that the relative error is very small and constant in the whole measurement range. At the same time, the design has great flexibility, high integration, with some reference value. Especially in the field of electronic design, where SOC technology has recently become increasingly mature, this design shows great significance.

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